from the memory array; and operating means that update the input address signal based on a control signal.

Please add the following new claims:

17. (Added) A semiconductor integrated circuit according to claim 2, wherein the storing means are a volatile memory.

18. (Added) A semiconductor integrated circuit according to claim 2, wherein the variable address converting means comprise: a memory array in which a plurality of memory cells are arranged in a matrix shape; an address decoder that selects the memory cells in the memory array based on an input address signal; reading means that amplify a signal read from the memory array; and operating means that update the input address signal based on a control signal.

19. (Added) A semiconductor integrated circuit according to claim 3, wherein the variable address converting means comprise: a memory array in which a plurality of memory cells are arranged in a matrix shape; an address decoder that selects the memory cells in the memory array based on an input address signal; reading means that amplify a signal read from the memory array; and operating means that update the input address signal based on a control signal.

20. (Added) A semiconductor integrated circuit according to claim 17, wherein the variable address converting means comprise: a memory array in which a plurality of memory cells are arranged in a matrix shape; an address decoder that selects the memory cells in the memory array based on an input address signal; reading means that amplify a signal read from the memory array; and operating means that update the input address signal based on a control signal.